

## ORGANIZATIONAL GUIDELINES

Welcome to Barcelona and to the HiPEAC Computing Systems Week! Let us describe some organizational procedures in order to make your stay more comfortable.

**Badge:** Please keep visible the accreditation you have been given at the registration desk during the events in order to identify all attendees as well as getting to know each other.

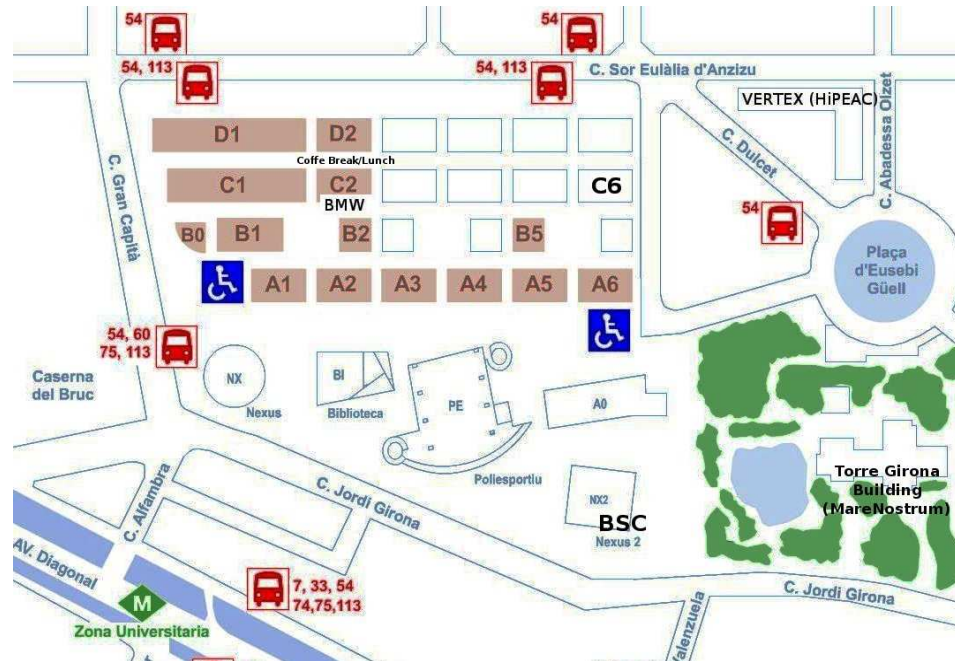
**Program:** Please refer to this leaflet in order to have further information about the events and locations.

### Meeting rooms:

- Monday and Tuesday, **Cluster Meetings:** Vertex building at basement theater "Sala Actes", basement meeting rooms VS2xx; and second floor rooms V2xx.
- Thursday and Friday, **BMW08:** at Sala d'Actes C2 building (ETSECCPB Civil Engineering School).
- Networking room: Computer Architecture Dept., C6-E106
- Sala del Llac is at the Torre Girona building.

### Coffee breaks and lunches:

- Monday and Tuesday: Vertex building garden.
- Thursday and Friday: between C2 and D2 buildings.



**MareNostrum visits:** BSC supercomputer tours will take place at the Torre Girona building. For security reasons, only groups of maximum 30 people will be allowed. There is room for one group on Monday at 19:00h. More groups can visit it on Thursday at 17:30h.

## 5th HiPEAC Industrial Workshop Information



- Hosted by **HP Labs**, at Sant Cugat del Vallès
- Address: Avda. Graells, 501, 08174 St. Cugat (Barcelona)
- All guests must be registered with HP security and wear a HP badge while at HP's premises. Bring your ID or passport.
- How to get there: If you are taking public transport from Barcelona, plan for the trip to last approximately 45 minutes. Instructions: [http://www.hipeac.net/system/files/hp\\_site.pdf](http://www.hipeac.net/system/files/hp_site.pdf). Location map: <http://tinyurl.com/5juqhn>.
- For HiPEAC Computing Systems Week attendees, buses leave from UPC Campus (Vertex Building) at 8 am. We will be back at 6:30 pm.

### Addresses at UPC Campus Nord:

**Edifici Vertex**  
Universitat Politècnica de Catalunya  
Plaça Eusebi Güell, 6  
08034 Barcelona

**Sala d'Actes C2 building, ETSECCPB**  
Jordi Girona, 1-3 , Edifici C2  
08034 Barcelona

**Barcelona Supercomputing Center**  
Nexus II Building  
c/ Jordi Girona, 29  
08034 Barcelona (Spain)  
Phone: (+34) 93 413 77 16

**To contact local organizers:**  
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# HiPEAC Computing Systems Week

June 2-6 2008  
Barcelona, Spain

<http://www.hipeac.net>



# HiPEAC Cluster meetings

## Monday 2nd

Time	Event	Location
12:00 – 13:30	Registration	Vertex Sala Actes
13:30 – 13:40	Welcome	Vertex Sala Actes
13:40 – 15:00	Multicores	Vertex Sala Actes
	ACOTES	Sala del Llac
	MILEPOST	C6-E101
15:00 – 15:30	Coffee break	Vertex Garden
15:30 – 17:00	Reconfigurable	Vertex Sala Actes
	Compilation Platform	Vertex S218
	Multicore-cont	Vertex S215
17:00 – 17:30	Break	
17:30 – 19:00	Virtualization	Vertex Sala Actes
	Task Force Low Power	Vertex S215
19:00 - 19:45	Visit to MareNostrum	Torre Girona
20:00 - 22:00	Reception	Temporada Rest.

## Tuesday 3rd

Time	Event	Location
8:30 – 10:00	Adaptive Compilation	Vertex Sala Actes
	Interconnects	Vertex S218
10:00 – 10:30	Coffee break	Vertex Garden
10:30 – 12:00	Programming models	Vertex Sala Actes
	Design Methodology	Vertex S218
	ACSEES	Vertex S215
	SARC WP2	Vertex S213
12:00 – 13:30	Lunch	Vertex Garden
13:30 – 15:00	Simulation Platform	Vertex Sala Actes
	Task Force Reliability	Vertex S218
	Task Force Education	Vertex S215
	SARC WP3	Vertex S213
15:00 – 15:30	Coffee break	Vertex Garden
15:30 – 17:00	Performance tools	Vertex 205
	SARC	Vertex 204
	HiPerf Real-time	C6-E101
17:00 – 17:30	Break	
17:30 – 19:00	SARC break-out	Vertex 205
	HiPEAC SC	Sala del Llac

# 5th HiPEAC Industrial Workshop

## Wednesday 4th

Time	Event
8:00	Bus Departure from UPC
8:30	Registration
9:15	Opening Remarks
9:30	Keynote: <i>Getting C++ threads right</i> , Hans Boehm, HP Labs
10:20	Break
10:45	- <i>Compiling C to CLI for Heterogeneous Multicore System-on-Chips: Erven Rohou, Andrea Ornstein, Marco Cornero</i>
Compilation and Code Generation	- <i>Programming Multicore Systems Using Hierarchically Tiled Arrays: Diego Andrade, James Brodman, Basilio Fraguela, David Padua</i>
	- <i>Polyhedral code generation for GPUs, by Piotr Lesnicki: Cedric Bastoul, Albert Cohen, DaeGon Kim, Louis-Noel Pouchet</i>
	- <i>Automating generation of data movement code for parallel architectures with distributed memories: Lee Howes, Anton Lokhmotov, Paul Kelly, Alastair Donaldson</i>
12:30	Lunch
13:30	- <i>COTSon: infrastructure for system-level simulation of clustered multicores: Eduardo Argollo, Ayose Falcon, Paolo Faraboschi, Daniel Ortega</i>
Tools	- <i>A Tool Environment for Data Locality Optimization on Chip-Multiprocessors: David Kramer, Oliver Mattes, Rainer Buchty, Wolfgang Karl</i>
	- <i>Clock Synchronization in Cell BE Traces: Marina Biberstein, Yuval Harel, Andre Heilper</i>
	- <i>A Dynamic Analysis Tool for Finding Coarse-Grain Parallelism: Sean Rul, Hans Vandierendonck, Koen De Bosschere</i>
15:15	Break
15:45	- <i>CAPSULE: A Symbiotic Hardware/Software Approach for Facilitating the Parallelization of Programs with Complex Control Flow and Data Structures: Olivier Certner, Zheng Li, Olivier Temam</i>
Methodology	- <i>MAPS: An Integrated Framework for MPSoC Application Parallelization: Weihua Sheng, Jeronimo Castrillon, Jianjiang Ceng, Hanno Scharwaechter, Rainer Leupers, Gerd Ascheid, Heinrich Meyr, Tsuyoshi Isshiki, Hiroaki Kunieda</i>
	- <i>On-chip memories, the OS perspective: Carlos Villavieja, Isaac Gelado, Alex Ramirez, N. Navarro</i>
	- <i>Overhead of the spin-lock loop in UltraSPARC T2: Vladimir Cakarevic, Petar Radojkovic, Francisco Cazorla, Robert Gioiosa, Mario Nemirovsky, Mateo Valero, Manuel A. Pajuelo Gonzalez, Javier Verdu</i>
18:00	Bus Departure to UPC

# BMW08 Barcelona Multicore Workshop

## Thursday 5th

Time	Event
8:30	Registration
9:00	<i>Welcome Talk</i> , Mateo Valero, BSC/UPC
9:10	<i>The Rock Architecture</i> , Marc Tremblay, SUN
9:40	<i>Future CPU Architectures: The Shift From Traditional Models</i> , Jesus Corbal, Intel
10:10	<i>Parallel Computing using NVIDIA CUDA</i> , Simon Green, NVIDIA
10:40	Coffee break
11:00	<i>Decoupled Composable Processors</i> , Doug Burger, Microsoft Research
11:30	<i>Programming Heterogeneous Multicore Processors</i> , Peter Hofstee, IBM
12:00	<i>Parallelizing Computer System Simulators</i> , Derek Chiou, UT-Austin
12:30	Lunch
14:00	<i>Design and Implementation of Transactional Constructs for C/C++</i> , Ali-Reza Adl-Tabatabai, Intel
14:30	<i>Making Transactional Memory More Scalable</i> , Maurice Herlihy, Brown U.
15:00	<i>Major Hurdles of Hardware Transactional Memory and Some Solutions</i> , Per Stenström, Chalmers U.
15:30	Coffee break
16:00	Panel "50 Billion Transistor Chips: What should the Hardware provide?", chaired by Yale Patt, UT-Austin

## Friday 6th

Time	Event
9:00	<i>European Research in Computing</i> , Panagiotis Tsarchopoulos, European Commission
9:30	Panel "What Terrifies You More: Multicore Hardware or Software?", chaired by Dan Reed, Microsoft
11:00	Coffee break
11:15	<i>StarSs: Portable Programming for a Fuzzy Multicore Space</i> , Jesus Labarta, BSC/UPC
11:45	<i>UPCRC at Illinois: Making Parallel Programming Synonymous with Programming</i> , Marc Snir, UIUC
12:15	<i>Towards Pervasive Parallelism: Parallel Applications without Parallel Programming</i> , Kunle Olukotun, Stanford U.
12:45	<i>Compiling for Multi, Many and Anycore</i> , Rudi Eigenmann, Purdue U.
13:15	Close